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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,344	12/29/2003	Kristopher J. Frutschy	42P17768	8138

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,344	FRUTSCHY, KRISTOPHER J.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5-8, 11, 17-19, 22-25, 34, 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsumura, US Patent No. 6,288,376 B1.

Tsumura anticipates limitations from claim 1, a method of coupling a semiconductor die with a next level package, comprising:

in figs. 10 and 11, providing at least one interconnect 21C; arranging the semiconductor die 210A, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package 2,

diagramed fig. 3A and 3B, generating an electromagnetic flux, illustrated by arrows, with an inductor 41A, 41B; and exposing the semiconductor die to the electromagnetic flux to induce eddy currents in the semiconductor die, wherein figs. 3A and 3B, illustrate the electromagnetic flux inducing eddy currents to produce heat, col. 6, lines 21-41, however, the flux is not isolated to just the interconnects, but rather radiates outward from the inductor to produce eddy currents and hence heat in all material within a range, including the semiconductor;

in figs. 10, 11, to heat the semiconductor die and couple the semiconductor die with the next level package, col. 9, line 4-38;

limitations from claim 17, a method wherein, in figs 3A and 3B, exposing the at least one interconnect to the electromagnetic flux to induce eddy currents in the at least one interconnect; to heat the at least one interconnect and couple the semiconductor die with the next level package, col. 6, lines 21-41;

limitations from claims 2, 18, the method, in figs. 10-11, wherein the heating preferentially heats the semiconductor die over the next level package, as the dies are closer to the inductors, col. 9, line 4-38;

limitations from claims 5, 22, the method, in figs. 1, wherein the at least one interconnect comprises an array of interconnects, 21a - 21d;

limitations from claim 6, 23, the method, in figs. 10-11, wherein the array of interconnects is formed on the semiconductor die 210A;

limitations from claims 7, 24, the method, in figs. 10-11, further comprising arranging the inductor such that the semiconductor die is interposed between the inductor and the next level package;

limitations from claims 8, 25, the method, figs. 10-11, wherein the next level package is a substrate 2;

limitations from claim 11, 28, the method, wherein the next level package is a printed wiring board, col. 1, lines 59-63;

limitations from claim 19, the method of claim 18, figs. 3A and 3B, wherein the heating preferentially heats the at least one interconnect 21c1, 21c2, over the semiconductor die, col. 6, lines 21-41;

limitations from claims 34-37, the method, in figs. 1-2, wherein exposing the semiconductor die to the electromagnetic flux to induce eddy currents in the semiconductor die comprises scanning the inductor around the semiconductor die, wherein in fig. 1, the inductor 42 scans in the direction of the arrow with the label MOVE, col. 7, lines 37-46.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, 13, 16, 29, 30, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura as applied to claims 1, 2, 5-8, 11, 17, 19, 24, 25, 34, 36 above.

While Tsumura does not illustrate all known configurations, the drawings are heuristic. Tsumura allows the practitioner to modify the device configuration as needed,

including limitations from claim 12, 29, the method, further comprising arranging the inductor such that the next level package is interposed between the inductor and the semiconductor die, col. 9, lines 39-45;

and limitations from claims 13, 30, the method, figs. 10-11, wherein the next level package can be another is a substrate, 2; or

limitations from claim 16, 33, the method, wherein the next level package is a printed wiring board, col. 1, lines 59-63;

Claims 3, 4, 20, 21, 35, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura as applied to claims 1, 2, 5-8, 11, 17, 19, 24, 25, 34, 36 above, and further in view of Luo et al., US Patent No. 6,379,576 B2.

Tsumura does not specify a pancake configuration or frequency of operation for his inductor, but Luo does. Luo teaches

limitations from claim 3, 20, the method, wherein generating an electromagnetic flux comprises providing an alternating electric current having a frequency exceeding 1 megahertz, col. 6, line 61 - col. 7, line 13;

limitations from claim 4, 21, the method, wherein generating an electromagnetic flux comprises providing an alternating electric current having a frequency of approximately 13.2 megahertz, col. 6, line 61 - col. 7, line 13;

limitations from claim 35, the method of claim 1, wherein the inductor is a pancake inductor, col. 6, line 61 - col. 7, line 13.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Luo's process with Tsumura's invention would have been beneficial because it gives the practitioner the choice of using a standard inductor configuration with one of the ISM harmonic frequencies, thus avoiding costly custom configurations.

Claims 9, 10, 14, 15, 26, 27, 31, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura as applied to claims 1, 2, 5-8, 11-13, 16, 17, 22-24, 29, 30, 33 above, and further in view of Fujii et al., US Publication No. 2003/0006489 A1.

Tsumura does not specify a flexible substrate or interposer, but Fujii does. Fujii teaches the method, wherein the next level package is a flexible substrate, wherein the next level package is an interposer, p. 1, ¶ 1. Fujii gives motivation in p. 2, ¶ 17. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Fujii's invention with Tsumura's invention would have been beneficial because the invention provides for very minute wiring conductors that can be easily formed.

Claims 38-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura in view of Luo.

Tsumura teaches limitations from claim 38, a method of coupling a semiconductor die with a next level package, comprising:

in figs. 10 and 11, providing at least one interconnect 21C; arranging the semiconductor die 210A, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package 2,

limitations from claims 39, diagramed fig. 3A and 3B, generating an electromagnetic flux, illustrated by arrows, with an inductor 41A, 41B; and exposing the semiconductor die to the electromagnetic flux to induce eddy currents in the semiconductor die,

limitations from claim 49, wherein figs. 3A and 3B, illustrate the electromagnetic flux inducing eddy currents to produce heat, col. 6, lines 21-41, however, the flux is not isolated to just the interconnects, but rather radiates outward from the inductor to produce eddy currents and hence heat in all material within a range, including the semiconductor;

in figs. 10, 11, heating the semiconductor die and couple the semiconductor die with the next level package, col. 9, line 4-38;

limitations from claims 40, 43, the method, in figs. 1-2, wherein exposing the semiconductor die to the electromagnetic flux to induce eddy currents in the semiconductor die comprises scanning the inductor around the semiconductor die, wherein in fig. 1, the inductor 42 scans in the direction of the arrow with the label MOVE, col. 7, lines 37-46.

Tsumura does not specify a pancake configuration or frequency of operation for his inductor, but Luo does. Luo teaches

limitations including, the method, wherein generating an electromagnetic flux with a pancake coil, col. 6, line 61 - col. 7, line 13.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Luo's process with Tsumura's invention would have been beneficial because it gives the practitioner the choice of using a standard inductor configuration with one of the ISM harmonic frequencies, thus avoiding costly custom configurations.

Response to Arguments

Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection. Tsumura teaches the inductor creating electromagnetic flux to produce eddy currents, and hence heat.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

4 August 2005
WB